31. (Amended) A memory cell, comprising:

a transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a second source/drain region having a first plate formed integral therewith, a body region and a [second] first source/drain region; and

a trench capacitor formed in a trench and electrically coupled without an intervening conductor to the first plate;

wherein the trench capacitor includes a polysilicon second plate formed in the trench that is coupled to the first plate of the second source/drain region, the first plate including a surface layer of polysilicon that is etch- roughened , and an insulator layer that separates the second polysilicon plate from the etch-roughened polysilicon surface of the first plate .

35. (Amended) A memory device, comprising:

an array of memory cells, each memory cell including [an] a vertical access transistor that is electrically connected without an intervening conductor to a trench capacitor by a first plate of the trench capacitor that is integral with a second source/drain region of the vertical access transistor, the first plate including a micro-roughened surface of porous polysilicon , with a second plate of the trench capacitor disposed so as to surround at least the micro-roughened surface of the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the vertical access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of vertical access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

36. (Amended) The memory device of claim 35, wherein the vertical access transistor includes a body region of p-type single crystalline silicon adjoining the second source/drain region, wherein the second source/drain region is n-type single crystalline silicon.

40. (Amended) The memory cell according to claim 35, wherein the second source/drain of the vertical access transistor is P-doped or N-doped.

41. (Amended) A memory cell, comprising:

a transistor comprising outwardly from a substrate a second source/drain region at least a portion of which serves as a single crystalline first capacitor plate for forming a conductorless connection of the transistor to a trench capacitor, a body region and a first source/drain region, wherein the first capacitor plate includes a micro-roughened surface for increasing the capacitance of the trench capacitor;

the trench capacitor being formed in a trench surrounding a portion of the [lateral] transistor and including a second capacitor plate of polycrystalline material formed so as to surround the first capacitor; and

an insulator layer that separates the second polycrystalline semiconductor plate from the micro-roughened surface of the first plate.

43. (Amended) [A] The memory cell according to claim 41, wherein the second source/drain region that includes the first capacitor plate, the body region, and the first source/drain region are formed as a pillar of single-crystal semiconductor material.

44. (Amended) [A] The memory cell according to claim 41, wherein the second plate also surrounds first plates of adjacent memory cells.

45. (Amended) [A] The memory cell according to claim 44, wherein the second plate is grounded.

46. (Amended) [A] The memory cell according to claim 17, wherein the first plate also surrounds second plates of adjacent memory cells.